A 4800-V Grid-Connected Electrical Vehicle Charging Station that Provides STACOM-APF Functions with A Bi-directional, Multi-level, Cascaded Converter

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Abstract— **This paper presents a new design for an ultra-fast, public electric vehicle (EV) charging station. Because of the multi-megawatt nature of such a station, the design is aimed at being appropriate for a medium voltage (MV) connection. Through the proper choice of a multi-level topology and staircase modulation, it is able to operate efficiently and provide galvanic isolation without the use of a large transformer. As a further benefit for this application, it is able to provide reactive, harmonic, and unbalanced load compensation. Simulation results are provided in Simulink to verify the effectiveness of the staircase modulation and capabilities of the topology.**

I. INTRODUCTION

In comparison to conventional road vehicles, electric vehicles (EVs) suffer from a limited range and long (>15 min.) charging times. It has been suggested [1] that the existence of public, ultrafast (≤3 min.) charging stations will address this issue to some extent. However, such stations have numerous challenges to overcome. For reasons of cost and multi-megawatt power levels, one challenge is to interface directly with distribution-level voltages (MV) while drawing an acceptable harmonic profile. For reasons of footprint and safety, a second challenge is to do this without a conventional (50/60 Hz) transformer while providing galvanic isolation for safety reasons. A final challenge is to address the negative impact that such stations are predicted to have on the electrical grid [1].

In addition to these challenges, there is a strong preference from utilities and investors to invest in new infrastructure and technology when it can provide multiple services or benefits in addition to its primary purpose. Because a charging station does not always operate at full power, this translates into several MVA of capacity that could be utilized (e.g., to provide reactive power support). Therefore, we have identified the following goals in addition to challenges discussed above: (1) the ability to compensate existing reactive, harmonic, and negative-sequence currents on the distribution system; (2) the ability to provide additional reactive support; and (3) the ability to provide load leveling (with the incorporation of a large battery or some other form of energy storage).

Existing topologies (for example, [1-7]) do not address all of these issues. In this paper, we present a modular design based on the isolated, DC-DC cell in [8]. These cells are connected and controlled in such a way to act as a MV, cascaded, multi-level inverter. Through an appropriate control and modulation scheme (described herein), our unique topology can draw arbitrary waveforms from the grid. This allows it to have STATCOM/APF and load-leveling capabilities to meet the goals above and to address its cost (both in capital expense and in negative impact on the grid). In addition, it draws current with an acceptable harmonic profile, is modular, provides galvanic isolation from the MV (4.8 kVrms, phase-phase or 3.92 kV) grid, and has a small footprint due to the absence of a 50/60 Hz transformer.

II. TOPOLOGY

A. Ultrafast Topology

We determined that the charging station (Fig. 1) should have a power rating of 2.4 MW (6 EVs, up to 400 kW each). In addition, we determined that the station should have an apparent power rating of 6 MVA to provide active and reactive power for grid support purposes. To achieve this MVA capacity and to achieve the current slew rate necessary for APF functionality, we determined that each phase should be able to produce +-4800 V and that the inductor L of each phase should be equal to 1 mH.

To minimize the charging station's impact on the grid during peak loading, we propose using a large battery or other form of energy storage for the common DC-link. This will enable EV charging without drawing power from the grid during those times. Because the topology is bi-directional, the battery can also be used to supply the grid during when the marginal cost of generation is very high.

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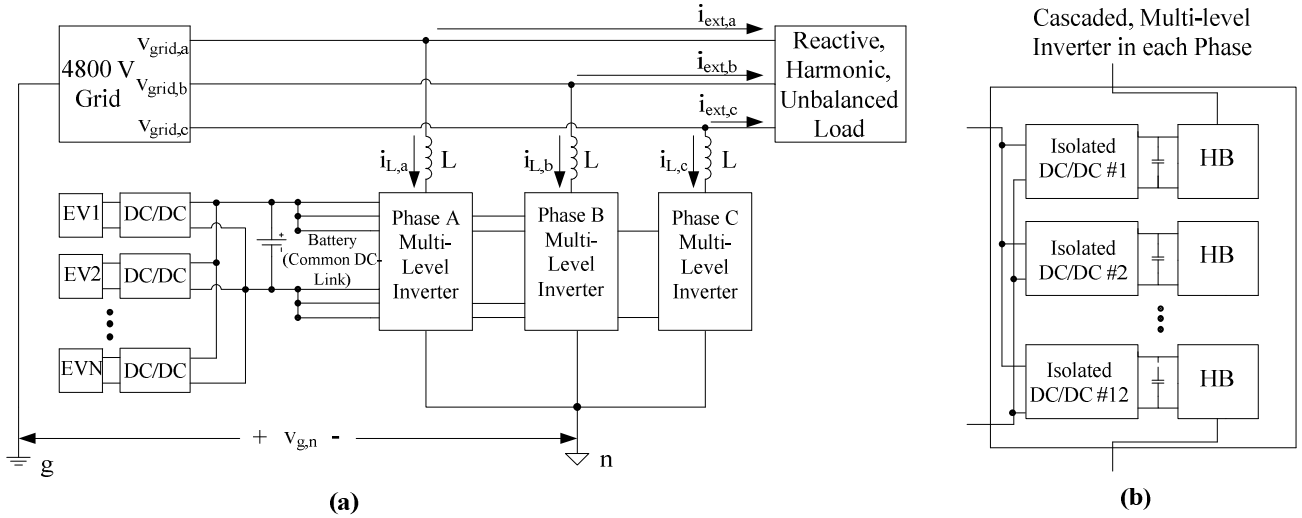

Figure 1: Layout of charging station with grid and load to be compensated (a) and the makeup of the multi-level inverter in each phase (b).

Our topology is u nique in that power flows through a common DC-link (see Fig. 1a) without the use of a bulky transformer. We have selected the cascaded H-bridge (HB), multilevel inverter of Fig. 1b as one of the best practical alternative to using a large transformer (SiC devices promise to fulfill this task with two-level inverters and enhanced efficiency in the future [9]). In particular we use 12, cascaded HBs per phase, each with a floating, 400V DC-link. Whether or not Si-C is used in future implementations to enhance the efficiency of our topology, multilevel modulation of the output voltage is optimal for this particular application because, as detailed in section V, it has vastly superior harmonic performance.

Finally, because of the modularity inherent in Fig. 1B, our topology is easily adapted to other voltages (say 7.2 or 13.8 kV). Alternatively, the HBs in Fig. 1B can be designed with higher DC-link voltages. The choice between these two alternatives depends on whether improving efficiency or harmonic performance is a priority.

B. Isolated, Bi-directional, DC-DC Converters and the Common DC-Link

As mentioned above, in our topology all power flows through the common DC-link. Key to this are the isolated, bi-directional, DC-DC converters shown in Fig. 1b. By virtue of the isolation, the DC-links in Fig. 1b can be stacked by the HBs while still being able to transfer energy to and from the common DC-link. [8] discusses a zero-voltage-switching (ZVS) converter that is a possible candidate for this application. As this paper focuses on the control of the output current and the necessary modulation of the HBs to achieve that, readers interested in the design and control of the isolated converters are directed to [8].

However, it is worth analyzing the benefit of a common DC-link. The total, instantaneous power drawn by a 3-phase load is constant in time for balanced, sinusoidal conditions. Therefore, when drawing/ supplying positive sequence current from/to the grid, our topology results in no low frequency power circulation in the battery (as shown in the simulation results). In theory, there are some other topologies that can draw a balanced, 3-phase power from MV levels and transfer it to a single DC load. However, they are unsuitable for this application because they either cannot function as a charging station [9], use a large transformer [1-3], draw unacceptable harmonics [4], have excessive capacitance requirements [1,3,5], do not provide galvanic isolation ([6] and [10]). Additionally, because the isolated, DC-DC converters are bidirectional and energy can be freely transferred between phases, our topology can correct any load imbalance upstream of it (as shown it Fig. 1a).

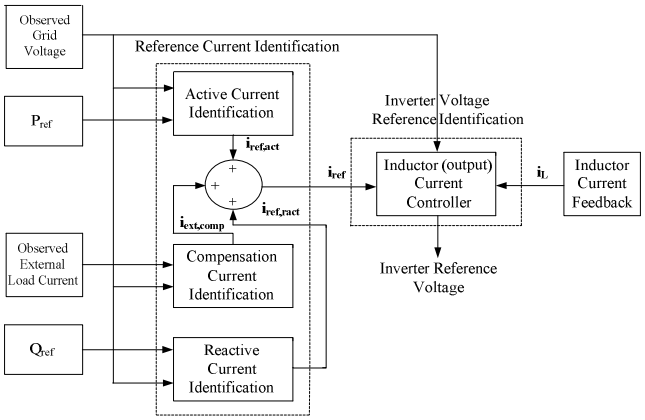

Figure 2: Overall control diagram showing how the reference current and then inverter reference voltage are determined.

III. REFERENCE CURRENT IDENTIFICATION

As shown in Fig. 2, the overall control process consists of two main steps which are the reference current identification (determining what current to draw from the grid) and the inverter voltage reference identification (the voltage

necessary to control i_{La}, i_{Lb}, and i_{Lc} in Fig. 1 so they follow the reference current). In this section, we develop a reference current identification scheme to achieve the following tasks: draw the appropriate amount of power to charge the EVs, charge/discharge the battery as commanded to provide grid support, provide APF/STATCOM compensation of the external load in Fig. 1a, and supply reactive power (in addition to that supplied by the STATCOM functionality) when commanded.

The first two tasks both require active power. Therefore, the first component of the inductor reference current is the active reference current and is a function of the reference power, P_{ref}. We use the following equation which, according to [14], calculates the active, positive sequence current necessary to draw P_{ref}:

$$\boldsymbol{i}_{ref,active} = \frac{\boldsymbol{v}_{grid} \cdot P_{ref}}{\boldsymbol{v}_{grid}^T \boldsymbol{v}_{grid}}, \tag{1}$$

where $\mathbf{v}_{grid}$ is the observed, three-phase, grid voltage column, $\mathbf{v}_{grid}{}^T\mathbf{v}_{grid}$ is the dot product of the grid voltage with itself, and bold is used to indicate a three phase column vector. P_{ref} is a function of the power demanded by the EVs and the power commanded to charge/discharge the battery. However, it is determined by a feedback controller and, so, is discussed in section IV.B.

Next we write the reference current to provide STATCOM/APF functionality. First, need to determine the component of the load current that we don't want to compensate. To do this, we adapt (1) to yield the active, positive-sequence current of the external load:

$$\boldsymbol{i}_{ext,active} = \frac{\boldsymbol{v}_{grid} \cdot P_{est,ext}}{\boldsymbol{v}_{grid}^T \boldsymbol{v}_{grid}}, \tag{2}$$

where $P_{est,ext}$ is the estimated, active power of the external load and is given by (6) and, again, bold indicates a three phase column vector.

Because the remaining components of the load current are what we wish to compensate, we write the compensation current reference as

$$\boldsymbol{i}_{ref,comp} = -\left(\boldsymbol{i}_{ext} - \boldsymbol{i}_{ext,active}\right) = \frac{\boldsymbol{v}_{grid} \cdot P_{est,ext}}{\boldsymbol{v}_{grid}^T \boldsymbol{v}_{grid}} - \boldsymbol{i}_{ext}, \tag{3}$$

where $\mathbf{i}_{ext}$ is the observed, external load current and the negative sign outside of the parentheses is due to the direction of the inductor current in Fig. 1a.

The final component of the reference current, is the component necessary to provide reactive support to the grid (in addition to reactive power supplied by compensating the external load). This is often desirable because supplying a net amount reactive power to the grid can help boost the voltage at a load bus. In order for the incoming inductor current to supply reactive power to the grid, the current needs to lead the grid voltage by 90˚. Therefore, (1) can be modified to give the equation for reactive current reference:

$$\boldsymbol{i}_{ref,reac} = \frac{\boldsymbol{v}_{grid}(t - 3/(4 \cdot f_{line})) \cdot Q_{ref}}{\boldsymbol{v}_{grid}^T \boldsymbol{v}_{grid}}, \tag{4}$$

where Q_{ref} is the reference command to supply reactive power to the grid and f_{line} is line frequency. Because Q_{ref} results in a balanced reactive power being supplied, this function does impose any extra requirements on or incur any losses in the battery.

Now that we have (1-3), we can combine them to form the equation for the total reference current of the inductors:

$$\begin{aligned} \boldsymbol{i}_{ref} &= \boldsymbol{i}_{ref,act} + \boldsymbol{i}_{ref,reac} + \boldsymbol{i}_{ref,comp} \\ &= \frac{\boldsymbol{v}_{grid} \cdot (P_{ref} + P_{ext,est}) + \boldsymbol{v}_{grid}(t - 3/(4 \cdot f_{line})) \cdot Q_{ref}}{\boldsymbol{v}_{grid}^T \boldsymbol{v}_{grid}} - \boldsymbol{i}_{ext} \end{aligned}, \tag{5}$$

where $P_{est,ext}$ is given by (6) and line frequency is 60Hz.

We discuss the determination of $P_{est,ext}$ last because it has a strong effect on APF/STATCOM performance. Various algorithms exist for this purpose with various trade-offs. We use the method developed in [11] which has an excellent trade-off between rapid transient response and robustness. It is also very simple:

$$P_{est,ext} = \frac{1\,\text{sec.}}{120} \int_{t-\text{sec.}/120}^{t} (\boldsymbol{v}_{grid}^T \boldsymbol{i}_{ext}) dt, \tag{6}$$

where $\mathbf{v}_{grid}{}^T\mathbf{i}_{ext}$ is dot product of the grid voltage and the external load current, and the integral is implemented with a moving average filter over the most recent half-cycle.

IV. Control and Modeling

A. Inductor Current Control

In order for the inductor current, $\mathbf{i}_L$, in Fig. 1a to follow the reference current, $\mathbf{i}_{ref}$, in equation (1), the correct voltage needs to applied to those inductors, and thus the correct inverter voltage $\mathbf{v}$ must be synthesized for each phase. Again, bold variables indicate a three-phase vector. To begin, we write the basic equation for the inductor current:

$$\frac{\mathrm{d}\boldsymbol{i}_{L,abc}}{\mathrm{d}t} = L^{-1}(\boldsymbol{v}_{grid} + v_{gn} - \boldsymbol{v}), \tag{7}$$

where $\mathbf{v}_{grid}$ is the three phase grid voltage, $\mathbf{v}$ is the three phase inverter voltage, and v_{gn} is the common mode voltage between the grid ground and the floating inverter neutral.

Since there is no neutral current, we do not desire there to be any neutral component in the reference current. Therefore, there will no neutral component in d**i**/dt. With this assumption, we can drop the ground to neutral voltage:

$$\frac{d\boldsymbol{i}_L}{dt} = \boldsymbol{L}^{-1}(\boldsymbol{v}_{grid} - \boldsymbol{v}), \tag{8}$$

We are now going to approximate di/dt as being constant in the next T_s seconds (Ts is sampling time period or the dead-beat delay time in dead beat control and is set to 1/2880 or .000347 sec. as described at the end of section V). Therefore, we write:

$$\frac{\Delta \boldsymbol{I}_L}{T_s} = L^{-1}(\boldsymbol{v}_{grid} - \boldsymbol{v}), \tag{9}$$

Now we assume that we want $\mathbf{i}_L$ to be $\mathbf{i}_{ref}$ at the end of this period. Therefore, $\Delta\mathbf{i}_L=\mathbf{i}_{ref}-\mathbf{i}_L$. Substituting this expression into (4) yields:

$$\frac{\boldsymbol{i}_{ref} - \boldsymbol{i}_L}{T_s} = L^{-1}(\boldsymbol{v}_{grid} - \boldsymbol{v}), \tag{10}$$

and isolating **v** yields

$$\boldsymbol{v}^{(*)} = \boldsymbol{v}_{grid} - L\frac{\boldsymbol{i}_{ref}^{(*)} - \boldsymbol{i}_L}{T_s}. \tag{11}$$

Equation (6) is the is inverter voltage necessary to make $\Delta\mathbf{i}_L=\mathbf{i}_{ref}-\mathbf{i}_L$. That is, $\mathbf{i}_L$ will equal $\mathbf{i}_{ref}$ at the end of each T_s interval. Whenever a discrete-time controller is used to make a first-order system (as ours is) have zero error after one switching cycle, it known as deadbeat control (although this definition can be modified for n^{th} order systems). However, as we are using a natural form of modulation (Section V), the controller runs in continuous time and, strictly speaking, is not deadbeat.

Notice that there are "(*)" operators in (6). This is because we need to modify the expression for **v**. As discussed in section V, to prevent multiple switching, we need to add a smoothing filter to the expression for **v**. This expression is given by:

$$\begin{aligned} \boldsymbol{V}(s) &= C_{smooth}(s)\cdot \boldsymbol{V}(s)^{(*)} \\ &= \frac{.053s}{7\cdot e-09\cdot s^2 + .053\cdot s + 1}\cdot \boldsymbol{V}(s)^{(*)}, \end{aligned} \tag{12}$$

where $C_{smooth}(s)$ has unity gain at its resonance frequency of 60 Hz and a Q of 1/20.

In addition to $C_{smooth}(s)$, we need to compensate $\mathbf{i}_{ref}$ so that the resulting $\mathbf{i}_L$ will not have a steady-state, phase error at 60 Hz due to the delay of T_s. Therefore, we compensate $\mathbf{i}_{ref}$ with a lead compensator:

$$\boldsymbol{I}_{ref}(s)^{(*)} = C_{lead}(s)\cdot \boldsymbol{I}_{ref}(s) = 1.413\frac{s+266}{s+534}\cdot \boldsymbol{I}_{ref}(s), \tag{13}$$

where $C_{lead}(s)$ has unity gain and a phase lead of 19.6° at 60 Hz and minimal effect on other frequencies.

Combining (6), (7), and (8) yields the final equation for the inverter voltage:

$$\begin{aligned} \boldsymbol{V}(s) = {} & \frac{.053s}{7\cdot e-09\cdot s^2 + .053\cdot s + 1} \\ & \cdot\left(\boldsymbol{V}_{grid}(s) - L\frac{1.413\frac{s+266}{s+534}\boldsymbol{I}_{ref}(s) - \boldsymbol{I}_L(s)}{T_s}\right) \end{aligned} \tag{14}$$

When this equation and L = 1 mH are used, the inductor current has the per-phase transfer function of

$$\begin{aligned} &\frac{\boldsymbol{I}_{L,phase}(s)}{\boldsymbol{I}_{L,ref}(s)} \\ &= \frac{s+266}{s+534}\cdot\frac{.075}{2.44e-9\cdot s^2 + 1.84e-5\cdot s + .053} \end{aligned} \tag{15}$$

B. Battery Power Flow Control Loop and System Model

Under normal circumstances, the power demanded by the charging EVs (hereafter refered to as $P_{dem,EV}$) should be matched by power flowing from the grid, through the multi-level inverters to the DC-link (hereafter called P_{ret}). However, because ultra-fast vehicle charging presents a very transient load (especially if pulse-and-burp methods [12] are employed), we use an integral controller to soften the transients presented to the grid. In addition, integral control ensures that P_{ret} is exactly equal to $P_{dev,EV}$. To achieve this we have

$$P_{ref}^{(*)}(s) = \frac{10}{s}\left(P_{dem,EV}(s) - P_{ret}(s)\right), \tag{16}$$

where the integral gain of 10 is chosen to yield dominant pole in (20).

Equation (16) contains "(*)" because it needs modification. It does not allow the common DC-link's battery to be discharged (for grid support) or charged back up. Instead, it ensures that, at steady state, the returned power will exactly match the power consumed by the EVs. Therefore, we modify the integrand of (16) to allow the returned power to be different from the power consumed by the EVs if desired:

$$P_{ref}(s) = \frac{10}{s}\left(P_{dem,EV}(s) - P_{ref,supp}(s) - P_{ret}(s)\right), \quad (17)$$

where $P_{ref,supp}$ is the reference power for grid support. When $P_{ref,supp}$ is negative, then the steady state value of P_{ret} will be greater than $P_{dem,EV}$. This discrepancy will flow into the battery causing the battery to be charged. Vice versa, when $P_{ref,supp}$ is positive, the battery will discharge providing grid support.

Because the relationship between P_{ref} and $\mathbf{i_L}$ is time-varying (1) and complicated (15), it is reasonable to first investigate the open-loop response of the system before further investigating the closed-loop performance. Therefore, equation below is based on open-loop simulation results. We used the same model described in the Simulation section except that we manually drove P_{ref} instead of using (17) to close the loop. Based on the open-loop step response of the observed P, we found the following pseudo-delay to be very accurate:

$$\frac{P(s)}{P_{ref}(s)} = \frac{1102}{s+1102}, \quad (18)$$

where P(s) is the actual resulting power drawn from the grid and the pole of $P(s)/P_{ref}(s)$ at s= -1102 corresponds to a time constant of 0.91 ms (i.e., it approximates a delay of 0.91ms).

To model the losses of the cascaded HBs and isolated converters (it is assumed that the dynamics of the isolated converters are fast enough so power flowing into them from the grid instantaneously appears at the battery), we assume a 97% efficiency [8]:

$$\frac{P_{ret}(s)}{P_{ref}(s)} = \frac{1102}{s+1102}\alpha(s), \quad (19)$$

where α(t) is 97% or 1/97% depending on the direction of power flow. This reciprocation happens because the bi-directional capability of the topology. When power flows from the DC-link to the grid, then P (the grid power) is 97% of P_{ret}. However, when power flows the other direction P_{ret} is 97% of P.

We can now substitute this equation into (17) and rearrange to yield

$$\frac{P_{ref}(s)}{P_{dem,EV}(s) - P_{ref,supp}(s)} = \frac{10(s+1102)}{s^2 + 1102 \cdot s + 11020 \cdot \alpha(s)}, \quad (20)$$

which, because $1 \approx \alpha(t) \approx \alpha(s)$, has a dominant pole at -10 rad./sec.

Because of the very dominant pole at -10 rad./sec., we can accurately model the power flow with the following approximations:

$$\begin{cases} \dfrac{P(s)}{P_{dem,EV}(s) - P_{ref,supp}(s)} = \dfrac{10}{s+10} \cdot \dfrac{1}{\alpha(s)} \text{ , or} \\ \dfrac{P_{ret}(s)}{P_{dem,EV}(s) - P_{ref,supp}(s)} = \dfrac{10}{s+10}. \end{cases} \quad (21)$$

Fig. 3a shows the response of the power absorbed from the grid to a 2.4 MW step in $P_{dem,EV}$ and a -5 MW step in $P_{ref,supp}$. Likewise, Fig. 3b shows the step-response of the power supplied by the battery based on (21). Comparing Fig. 3 to Fig. 10 in the simulation section shows that (21) is indeed an accurate approximation.

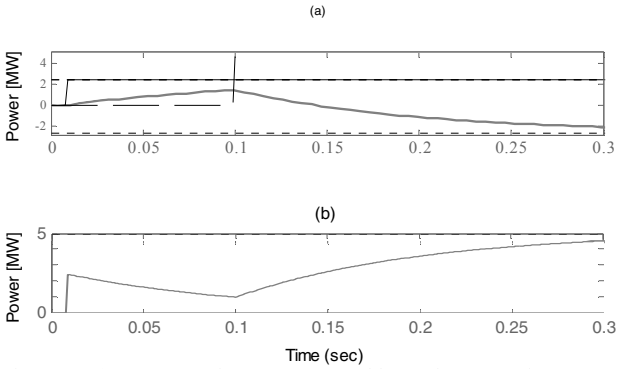

Figure 3: (a) Response of power consumed by station (gray) in response to step changes in EV charging power (solid) and grid support (dashed) according to equation (21) and (b) response of power supplied by battery.

C. Controller Limitations

In subsection A, we had to place some restrictions on (11) to arrive at (14). As discussed in more detail in the next section, this is because we are using a natural method to modulate the inverters and the reference voltage given by (11) contains frequency components near the switching frequency. Therefore, there is no guarantee that the average output voltage will equal the average reference voltage over a fixed interval T_s (the dead-beat delay time in (11)). This is especially apparent in Fig. 4 between t=45 ms and 47 ms.

These limitations, however, are not a fundamental limitation of our topology. Equation (11) could be used if a modulation method existed that could guarantee the average inverter output voltage is equal to a reference value over fixed, discrete-time intervals. Such a method, known as multi-level, space vector PWM (SVPWM) is the subject of Ch. 12 of [7]. While its implementation is far more complex than the staircase modulation we use in section V, the end result is very similar. Essentially, the only difference is that the edges of the output voltage in Fig. 4 timed to achieve a given average value. The rising and falling still happens in the same sequence.

To fully optimize the operation of the topology, we recommend the use of multi-level, SVPWM and synchronous, DQ-based, dead-beat controller. This will allow the bandwidth of dead-beat control to be achieved, without having a phase delay for the 60 Hz component [13] and without having to sacrifice the advantages of multi-level modulation discussed in the next section.

V. MULTILEVEL, STAIRCASE MODULATION OF THE CASCADED HBS

To synthesize the inverter output voltage determined in section IV.A, we use a type of naturally-sampled modulation called staircase modulation (investigated in [15]). This is shown in Fig. 4, where the inverter voltage follows the reference voltage in discrete, 400V steps. To achieve this, the cascaded HBs in Fig. 1b are switched on in sequence to stack the DC-links voltages. The exact time at which a new HB switches on is when the reference voltage crosses the halfway point between two, discrete, 400 V level. Thus, the first HB switches on when reference voltage reaches 200 V. In this way there are 48 steps per 60-Hz cycle (generating a full scale 4800 V magnitude output voltage) for an effective switching of F_s=2880 Hz.

Besides allowing interface with voltages much higher than the device ratings, there are several other advantages of using a multilevel inverter over a two-level inverter. First and foremost, the di/dt of the ripple is inversely proportional to N, the number of levels in the inverter (Figs. 11.6 and 11.7 of [7]). However, the achievable current slew rate is not reduced because the output voltage in Fig. 4 is free to make more than one level transition at a time. Therefore, for a given switching speed, the ripple current magnitude is reduced by the same factor. With a two-level inverter, this is accomplished by increasing switching speed, but this does not decrease the di/dt in the ripple current. Alternatively, an LCL output filter can be used but this requires complex control and a higher switching speed, for the same bandwidth. Therefore, our use of a 13-level inverter vastly improves the harmonics of the output current without sacrificing transient response or bandwidth while allowing negligible switching losses and a small inductor size!

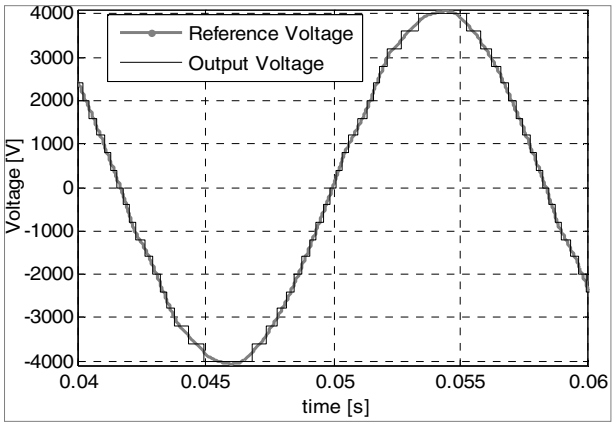

Figure 4: Phase A multi-level inverter output and reference voltages.

Another advantage of synthesizing the reference voltage in multiple steps is that it allows the use of the class of IGBTs with the lowest conduction losses. Typical devices (such as the IRG4PC50S) achieve forward voltage drops as low 1.1V but sacrifice the ability to switch faster than 1 kHz, preventing most PWM applications from exploiting their exceptional efficiency. However, they are very well suited for our topology because, as Fig. 4 shows, the topology enables an accurate synthesis of a reference waveform while on require each HB to change state 4 times per cycle.

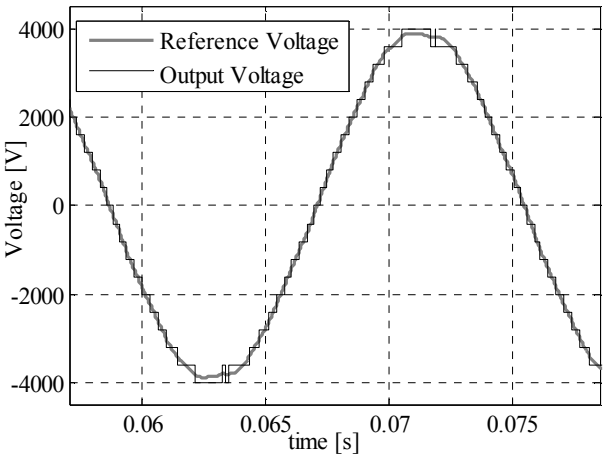

Figure 5: Phase A reference and output voltage while exhibiting multiple switching

Fig. 5, however, shows an issue that must be addressed. Thus far in our implementation of staircase modulation, there is nothing to prevent the multiple switching shown at t=.063s . In a worst-case scenario, the reference voltage can dither at high frequency about the midpoint between two voltage levels, resulting in improper synthesis of the reference voltage. This can be addressed by using comparators with hysteresis. However, this degrades the accuracy of the synthesis of the reference voltage, and (7-15) were developed on the assumption that **v** of (14) is accurately synthesized. Instead, we use a smoothing filter, $C_s(s)$, as discussed in section IV. A to help prevent dithering in reference waveform and an algorithm intercept multiple switching and freeze the HB's state for predetermined amount of time. Either way, the price of using staircase modulation is reduced bandwidth compared to what is theoretically achievable with our topology.

There is another shortcoming of the staircase modulation method. Essentially, it does not optimally time its rising and falling edges when the slope of the reference voltage is non-constant. By Examining Fig. 4 between t=45 ms and 47 ms, one can see that there is no guarantee that the resulting output voltage has the same average value as that of the reference voltage during this time period. As discussed in detail in section IV, Multilevel, SVPWM can be used to address this issue as well as the multiple switching issue without requiring a smoothing filter. Additionally, by pairing SVPWM with a DQ-based controller the topology can achieve the maximum theoretical bandwidth of 1440 Hz (F_s/2).

VI. SIMULATION

A. Simulink Model

We simulated our topology and control system in Simulink using the SimPowerSystems add-on as shown in Fig. 6. For the multilevel inverters, ideal voltage sources are used (as we are not modeling the dynamics of the isolated DC-DC converters). However, we do model the structure of Fig. 1B as being 97% efficient, as in (19).

The other blocks in the figure are the power reference block, reference current identification, the current controller, the grid, the EV load, and the external load. The power

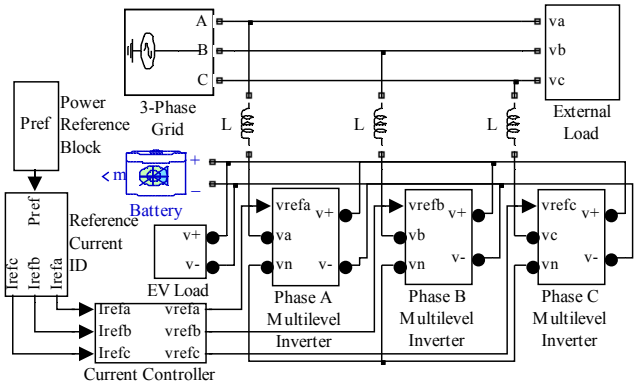

Figure 6: Simulink model.

reference block uses equation (17) to generate P_{ref}. The Pref signal and several other inputs are fed into the reference current identification block which uses (5) to generate $\mathbf{i}_{ref}$. The current control block uses (14) to generate the appropriate reference voltage, $\mathbf{v}$, to control the inductor current to follow $\mathbf{i}_{ref}$. The EV load models the power consumed by the EVs by drawing an appropriate amount of current from the battery.

B. Simulation Results for the Output Current and Compensation Effectiveness

To verify the transient and harmonic performance of the current control (14), we ran the following simulation: initially, the external load is drawing reactive, unbalanced, and harmonic currents (Fig. 7a, dashed curve), and then a 1 MW charging load is added at 0.05 sec. The phase A currents during this time are shown in Fig. 7. The dashed curve indicates that the load current has some harmonics and is out of phase with the grid voltage. The addition of the 1 MW charging load is indicated by the change in grid (solid curve) and charging station current (thick gray curve) after 0.05 sec. but no change in load current. The power flow during this time is shown for various parts of the system in Fig. 8.

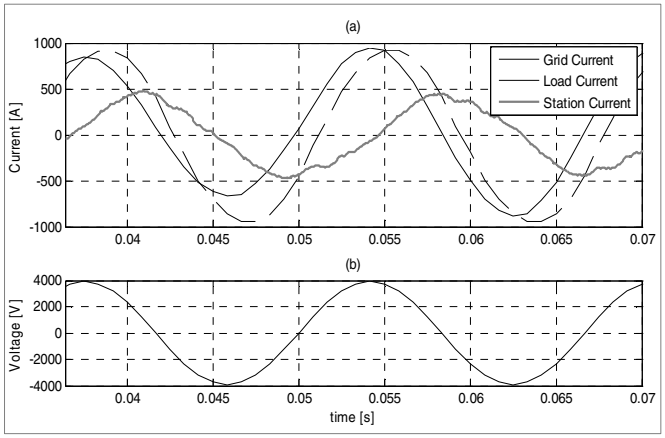

Figure 7: Phase A grid, charging station, and external load currents (a) and phase A grid voltage draw as a phase reference.

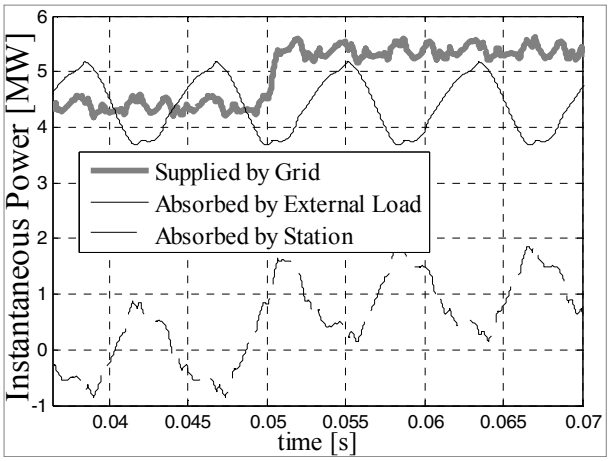

Figure 8: Instantaneous power supplied by the grid, absorbed by the external load, and absorbed by the charging station during simulation.

As the grid current (Fig. 7a) shows, the load current has been compensated so that the grid current is in phase with the voltage (plotted in Fig. 7b for reference). Thus the RMS current has been significantly reduced (Table I). As Table I shows, the overall harmonics have been reduced as well.

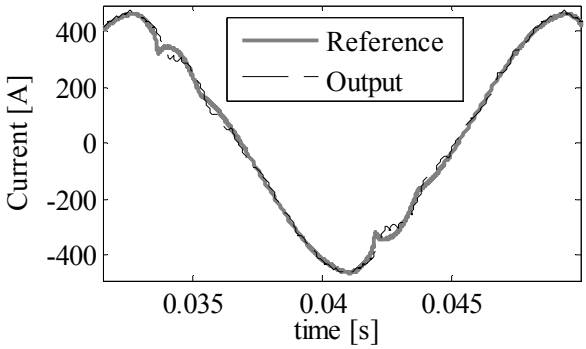

Figure 9: Output current (black) following phase A reference current (thick, gray).

The effectiveness of (14) can be verified visually as well. To do this, the phase A output current is compared to its reference in Fig. 9 when there is high harmonic content in the reference. Due to the limitations of our current control and modulation methods in section IV.C and the end of section V, there are some imperfections in the reference following. Overall, however, the figure indicates a decent ability to follow harmonics and transients.

C. Simulation Results of the Power Flow

Simulation was also used to verify (21), the system model of the power flow. In section IV, it was claimed that a dominant pole was introduced such that (21) becomes a very accurate approximation. To verify this we simulated the system with the same step changes in $P_{ref,EV}$ and $P_{ref,supp}$ that were used to generate Fig. 3. Comparing the power flow response of the full simulation model, Fig. 10, to Fig. 3 shows that (21) is indeed accurate.

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Table I: Simulation Results Summary

	Active Phase Current (RMS)	Current THD	Phase Current RMS	Total PF	Total Apparent Power	Total Active Power
External Load	523	2.76%	680	77%	5.6 MVA	4.3 MW
Grid Current w/o EV Charging	523	2.19 %	523	>99%	4.3 MVA	4.3 MW
Grid Current with EV Charging	648	1.2%	648	>99%	5.3 MVA	5.3 MW

system with the same step changes in $P_{ref,EV}$ and $P_{ref,supp}$ that were used to generate Fig. 3. Comparing the power flow response of the full simulation model, Fig. 10, to Fig. 3 shows that (21) is indeed accurate.

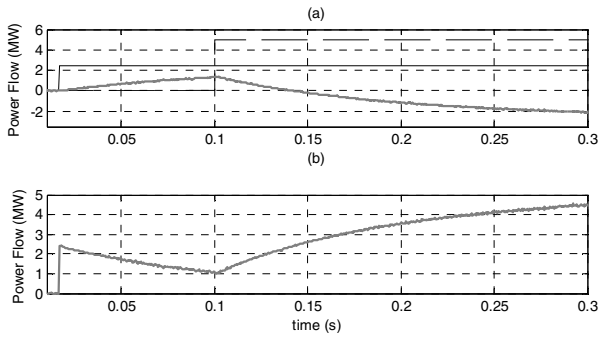

Figure 10: (a) Simulated response of power consumed by station (gray) in response to step changes in EV charging power (solid) and grid support (dashed) and (b) response of power supplied by battery.

VII. CONCLUSIONS

Because of the unique features of our topology (high power density, MV-level interface, excellent harmonic performance, and STATCOM/APF capabilities) it is ideally suited (from a utility point of view) for a public, ultra-fast, EV charging station. As the simulation results show it is capable of removing correcting a typical distribution load to 99% power factor (including harmonic, reactive, and negative-sequence currents). With the inclusion of the battery as the common DC-link, the charging station can operate without drawing power from the grid during heavy loads. In fact, with the bi-directional capability of the topology, the battery can be used to support the grid at strategic times.

As shown in section V, each H-bridge only changes state 240 times per second even though the effective switching frequency is 2880 Hz. This drastically reduces switching losses. With the use of staircase, multi-level modulation, we are able to achieve the bandwidth necessary to compensate harmonics while having small di/dt in the ripple current. However, as the bandwidth is still somewhat limited (15), any improvement in it is very valuable in this application. Theoretically, a 1440 Hz bandwidth should be achievable. Through the use of multi-level, SVPWM in conjunction with a DQ-based, dead-beat controller this can be realized.

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